a logic component (8) which is included in the integrated circuit (1) to be tested.

2. (Currently amended) [An arrangement as claimed in claim 1, characterized in that the integrated circuit (1) to be tested includes] The integrated circuit of claim 11, wherein the means for receiving test results comprises a test response analysis unit [(5)] for compressing test response vectors, [and] the integrated circuit further comprising a test control block [(6)] for controlling the test procedure.

3. (Cancel) An arrangement as claimed in claim 1, characterized in that the test vector generator (4) in the test system (2) is arranged to generate the test vectors that are intended to be transferred to the integrated circuit (1) to be tested.

4. (Currently amended) [An arrangement as claimed in claim 1, characterized in that the] The tester of claim 10, comprising a [test response analysis unit [(5) is included in the test system (2) and is] arranged to compress [the] test response vectors [to be] received from the integrated circuit [(1)] to be tested.

5. (Currently amended) [An arrangement as claimed in claim 1, characterized in that the test system (2) includes] The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator [(4)] which includes an arithmetic and logic unit [(ALU)] and generates test vectors in real time.

6. (Cancel) A method of testing logic circuits wherein test vectors that are generated by a programmable algorithmic test vector generator (4) which is included in a test system (2) are transferred to a circuit (1) to be tested which includes a logic component (8) to be tested, and wherein the test response vectors are compressed by means of a test response analysis unit (5) and the compressed test response vectors are evaluated by the test system (2).

7. (Cancel) An integrated circuit (1) which includes a test response analysis unit (5) and a test control block (60, wherein a circuit (1) to be tested is arranged to receive test vectors which are generated by a programmable algorithmic test vector generator (4) which is included in a test system (2), and to generate test response vectors, the test response analysis unit (5) being arranged to compress the test responses under the control of the test control block (6).

8. (Cancel) A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

9. (Cancel) A test system as claimed in claim 8, characterized in that a test response analysis unit (5) for compressing test response vectors supplied by the circuit (1) to be tested is integrated in the test system (2) which evaluates the compressed test response vectors.

10. (New) A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. (New) An integrated circuit comprising:

means for receiving from an external tester test vectors for the logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

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12. (New) A method of testing logic circuit of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. (New) The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further comprising the test response analysis unit:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.